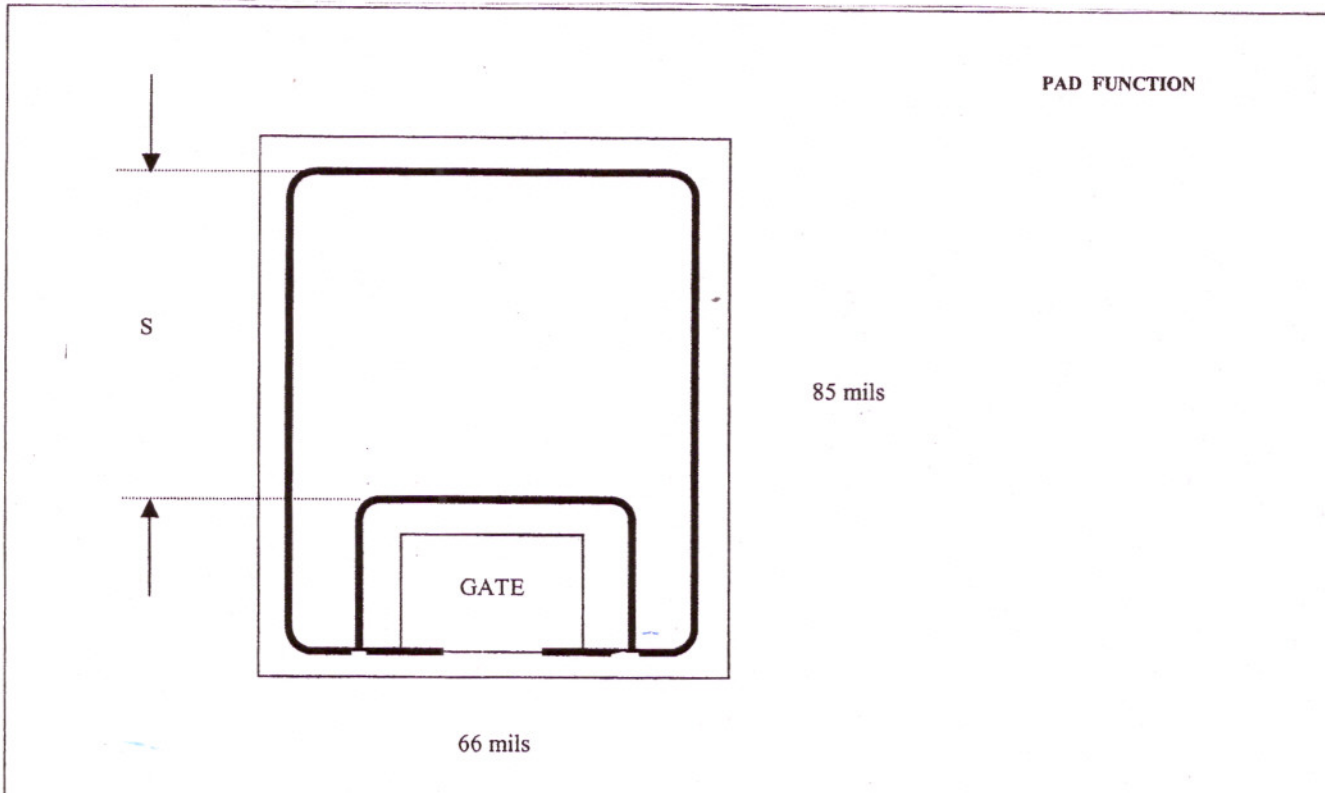




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CHIP BACK IS DRAIN

GATE = 20 x 25 mils. SOURCE CONNECTION CENTRALLY BETWEEN INDICATOR LINES (50 mils)

The information given is believed to be correct at the time of issue.

Please verify your requirements prior to commencement of any assembly process, as no liability for omission or error can be accepted.

Chip back potential is the level at which bulk silicon is maintained either by bond pad connection or in some cases the potential to which the chip back must be connected if stated above.

Note: 1 mil = 0.001inch

<p><u>APPROVED</u></p> <p>D Markham</p> <p>DATE: 23/05/02</p>	<p style="text-align: center;">IRFC024NB</p> <p style="text-align: center;">INTERNATIONAL RECTIFIER</p>	<p><u>DIE INFORMATION</u></p> <p>DIMENSIONS (Mils): 66 x 85 x 12 BOND PADS (Mils): G = 20 x 25 MASK. REF: GEN 5 GEOMETRY: BACK POTENTIAL: DRAIN</p>
<p><u>SERIAL NUMBER</u></p> <p>003649</p>		<p><u>METALLISATION</u></p> <p>TOP: Al BACK: CrNiAg</p>